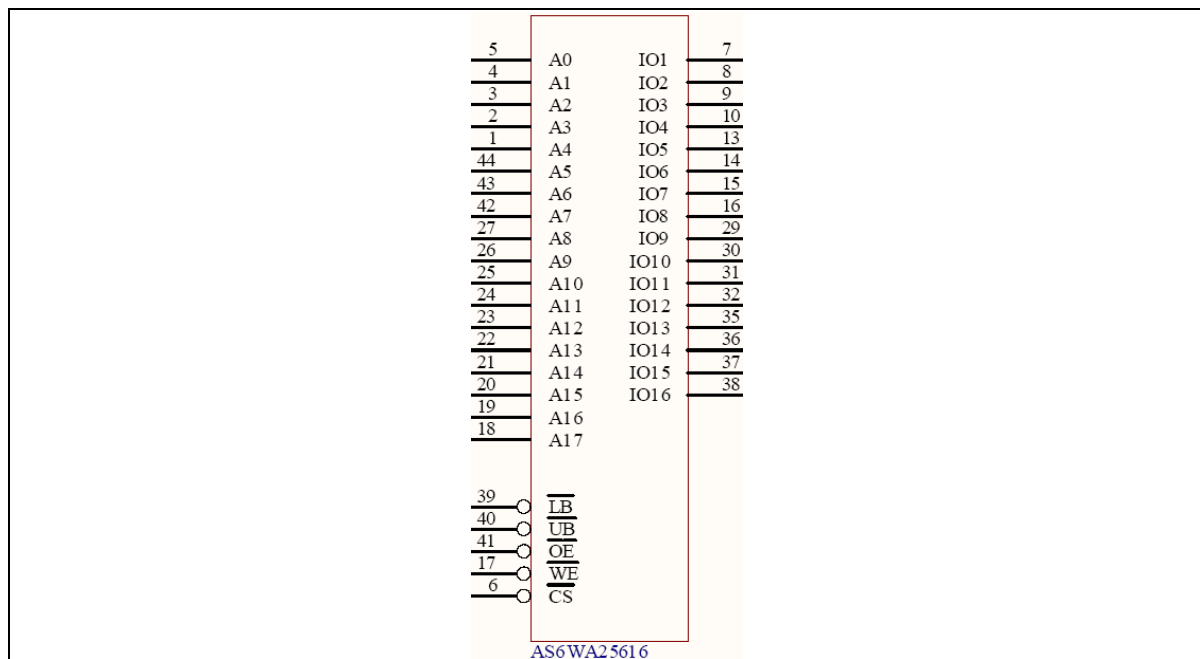


# Tutorial 11: Bus Memory Interface

## Problem 1: Processor Memory Interface with 16-bit Memory Module

The DSLMU board is augmented to a 256K × 16-bit read/write SRAM module that interfaces to the microcontroller through the external bus. This memory is where user instructions and data go. Draw a Picture of the interface between the memory module and the Processor.

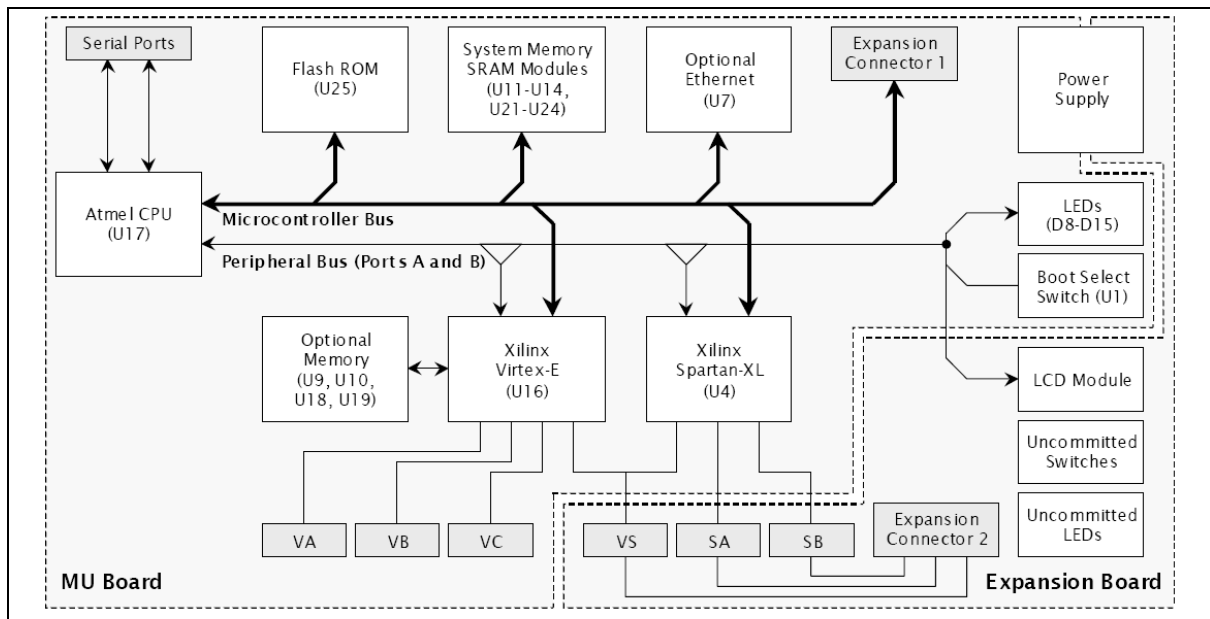
The pin layout of the memory module is shown in Figure 1.



**Figure 1: The pin layout of 256K × 16-bit memory modules**

Before we decide on the interface we need to look more carefully into the layout of this chip. We identify 18 address lines (A0 - A18) and 16 data lines (IO1 - IO16), which implies a SRAM configuration of  $2^{19} \times 16\text{-bit} = 256\text{K} \times 16\text{-bit} = 512\text{ Kbytes}$ . With 16-bit data interface, in each memory transaction only two bytes are transferred between the memory and the processor. However, ARM instructions are 32-bit size. That requires two transactions to memory for each instruction (or load and store data associated with LDR/STR instructions).

Furthermore, as we note from Figure 2, multiple devices are connected to the external bus.



**Figure 2: System Block Diagram for the DSLMU Board**

In order to ensure that only one external device takes part in memory transaction with the processor, the intended memory device is selected by asserting its “\CS” (Chip Select pin). If “\CS” is not asserted the data pins IO1 - IO16 are placed in High Impedance (Z) state; that is effectively disabled. Furthermore, the “read” operation is identified by the assertion of “\OE”, and the “write” operation by the assertion of “\WE”.

The memory interface also has two additional pins “\LB” and “\UB”. They refer to access to “Lower Byte” and “Upper Byte”. For normal 2-byte accesses both these pins need assertion. However, in byte accesses associated with LDRB/STRB instructions only one of these signals are asserted and only data lines IO1 - IO8 or IO9 - IO16 are used. The other data lines are placed in High Impedance (Z) state. Figure 3 summarises the functional description of the memory chip from its data sheet.

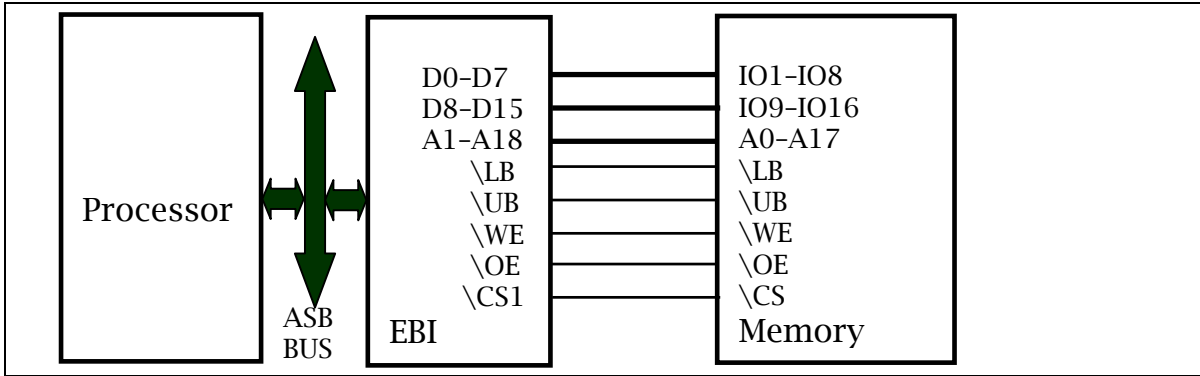
Truth table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{IB}$	$\overline{UB}$	Supply Current	I/O1-I/O8	I/O9-I/O16	Mode
H	X	X	X	X	$I_{SB}$	High Z	High Z	Standby ( $I_{SB}$ )
L	X	X	H	H	$I_{CC}$	High Z	High Z	Output disable ( $I_{CC}$ )
L	H	H	X	X	$I_{CC}$	$D_{OUT}$	High Z	Read ( $I_{CC}$ )
L	H	L	L	H	$I_{CC}$	High Z	$D_{OUT}$	
L	H	L	L	L	$I_{CC}$	$D_{OUT}$	$D_{OUT}$	
L	L	X	X	X	$I_{CC}$	$D_{IN}$	High Z	Write ( $I_{CC}$ )
L	L	X	H	L	$I_{CC}$	High Z	$D_{IN}$	
L	L	X	L	L	$I_{CC}$	$D_{IN}$	$D_{IN}$	

Key: X = Don't care, L = Low, H = High.

**Figure 3: Truth Table Description of the Memory Chip Control and IO Pins**

Figure 4 illustrates the Microcontroller Memory Interface.

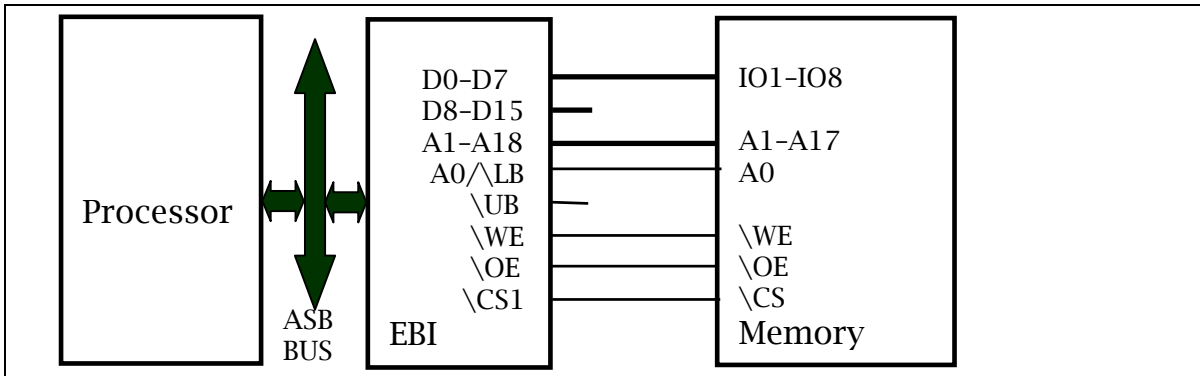


**Figure 4: The Interface Between the Microcontroller External Bus Interface (EBI) and 16-bit wide Memory**

### Problem 2: Processor Memory Interface with 8-bit Memory Module

The 256K × 1 6-bit read/write SRAM module on the DSLMU board is replaced with a 512K × 8-bit read/write SRAM module that interfaces to the microcontroller through the external bus. Draw a Picture of the interface between the memory module and the Processor.

Figure 5 illustrates the Microcontroller Memory Interface.



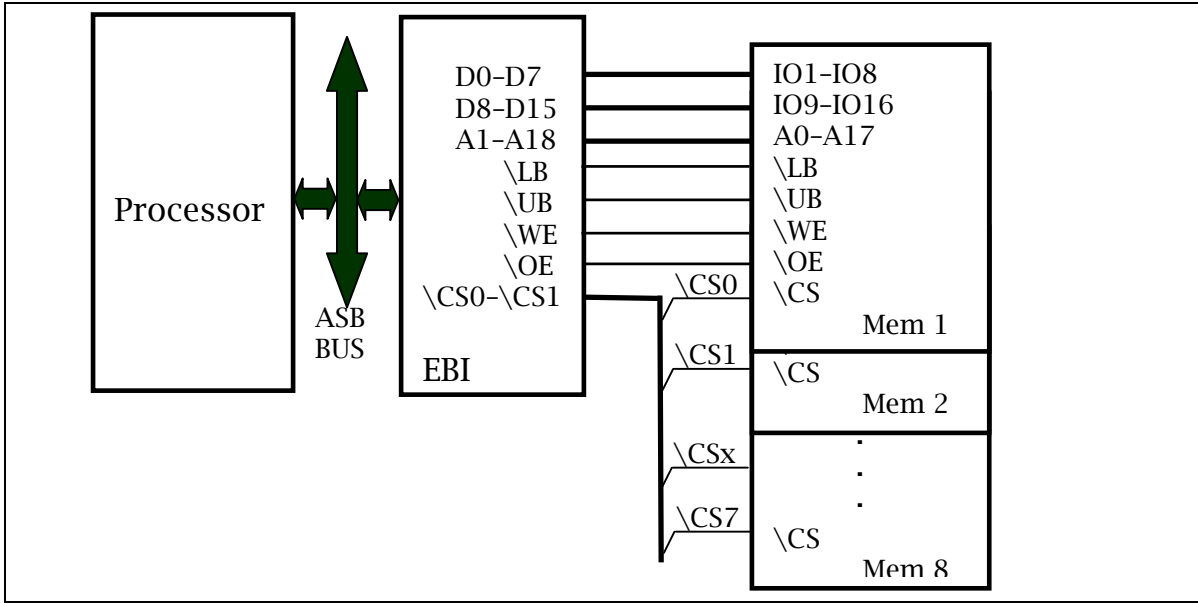
**Figure 5: The Interface Between the Microcontroller External Bus Interface (EBI) and 8-bit wide Memory**

With 8-bit data interface, in each memory transaction only one byte is transferred between the memory and the processor. However, ARM instructions are 32-bit size. That requires four transactions to memory for each instruction (or load and store data associated with LDR/STR instructions). That means that the processor speed reduces by at least a factor of 2.

### Problem 3: Processor Memory Interface with Multiple 16-bit Memory Modules

The DSLMU Hardware Reference Manual states that “Connected to the Microcontroller Bus is the system memory in the form of Static RAM modules, U11-U14 and U21-U24 providing up to eight 256K × 16-bit memory modules for a total of up to 4 MB of read/write memory. Draw a Picture of the interface between the memory modules and the Processor.

Figure 6 illustrates the Microcontroller Memory Interface.



**Figure 6: The Interface Between the Microcontroller External Bus Interface (EBI) and 8 Memory Modules with 16-bit Wide Data**

All the eight 256K × 16-bit memory modules Figure 6 share the same data lines (IO1 - IO16), address lines (A1 - A17), \WE, \OE, \LB, and \UB lines. However, each memory module is controlled by a different \CS line. \CS0 - \CS7 are mapped to a different regions of memory, which can be organised as contiguous regions or non-adjacent.