

# Tutorial 13: Virtual Memory

## Problem 1: Virtual Memory with Paging

Consider a memory system with 32-bit Virtual Address and 2 KB pages and 16-bit physical address. Determine the number of bits in the fields corresponding to the Virtual Pages Number, Page Offset, and Physical Page Number. Also determine the number of bits in each Page Table entry.

Page Offset:

2 KB page corresponds to 11 bits for Page Offset ( $2^{11} = 2\text{KB}$ ).

Virtual Page Number:

$32 - 11 = 21$ . That is there  $2^{21} = 2$  Mega of virtual pages.

Physical Page Number:

$16 - 11 = 5$ . That is there  $2^5 = 32$  physical pages.

Figure 1 identifies the fields in the Physical and virtual pages.

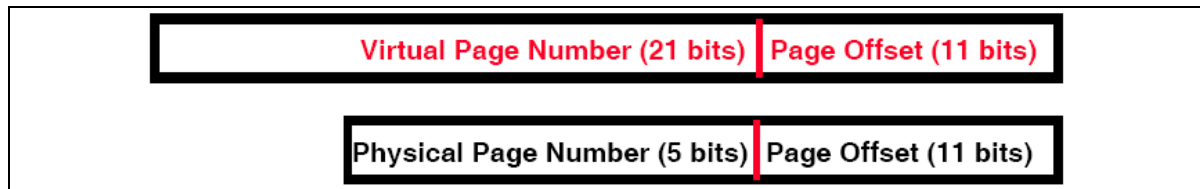


Figure 1: Identification of Fields in Virtual and Physical Addresses

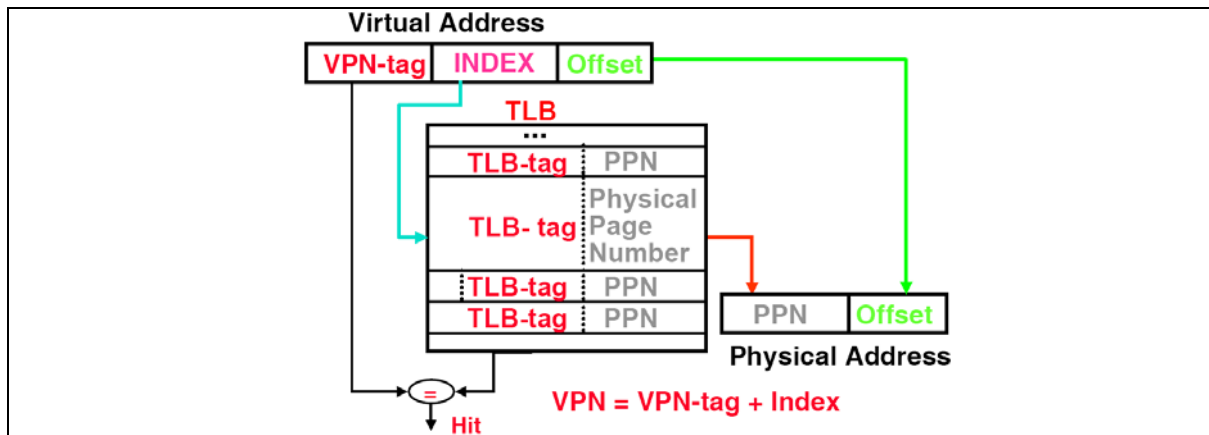
Page Table Entry Number:

(The number of bits in each Page Table entry) = (Number of Physical Page Number) + (Number Access Bits) + (Valid bit) + (dirty bit) =  $5 + 3 + 1 + 1 = 10$  bits

## Problem 2: Data Access in TLB

Consider a memory system shown in Figure 2, with 32-bit Virtual Address and 4 KB pages and 18-bit physical address. Determine the number of bits in the fields corresponding to the Virtual Pages Number, Page Offset, and Physical Page Number. If the TLB is 2-way set associative with 32 sets, compute the number of bits in TLB index, TLB VPN-tag and approximate number of bits in each TLB entry.

The memory system is also augmented with a 2K Byte, 16-Byte block, 2-way set associative cache that operates on physical addresses. Compute the number of bits in the offset, index, tag and the total number of bits in each cache entry.



**Figure 2: Organisation for 32 Set 2-Way Set Associative TLB**

Page Offset:

4 KB page corresponds to 12 bits for Page Offset ( $2^{12} = 4KB$ ).

Virtual Page Number:

$32 - 12 = 20$ . That is there  $2^{20} = 1$  Mega of virtual pages.

Physical Page Number:

$18 - 12 = 6$ . That is there  $2^6 = 64$  physical pages.

TLB Index:

From Figure 2 we can see that to select one out of 32 sets we need 5 bits for the TLB Offset.

TLB-Tag Number:

(The TLB-Tag Number) =  $32 - (\text{TLB Index}) - (\text{Offset}) = 32 - 5 - 12 = 15$  bits

TLB Entry Number:

(The number of bits in each TLB entry) = (Number of Physical Page Number) + (Number of TLB-Tag) + (Number Access Bits) + (Valid bit) + (Dirty bit) + (LRU bit) =  $6 + 15 + 3 + 1 + 1 + 1 = 27$  bits

Cache Offset Number:

Cache Offset =  $\log_2[\text{Block size}] = \log_2[16] = 4$  bits

Cache Index Number:

Cache Index =  $\log_2[(\text{Cache Size}) / ((\text{Block size}) \times (\text{Blocks per Set}))] = \log_2[(2K \text{ Byte}) / (16) \times (2)] = 6$  bits

Cache Tag = (Physical Address Number) - (Cache Index) - (Cache Offset) =  $18 - 6 - 4 = 8$

Cache Entry Number:

(The number of bits in Cache entry) = (Tag Number) + (Block size) + (Valid Bit) + (Dirty bit) + (LRU) =  $8 + 16 \times 8 + 1 + 1 + 1 = 135$  bits