

Tutorial 12: Cache

Problem 1: Direct Mapped Cache

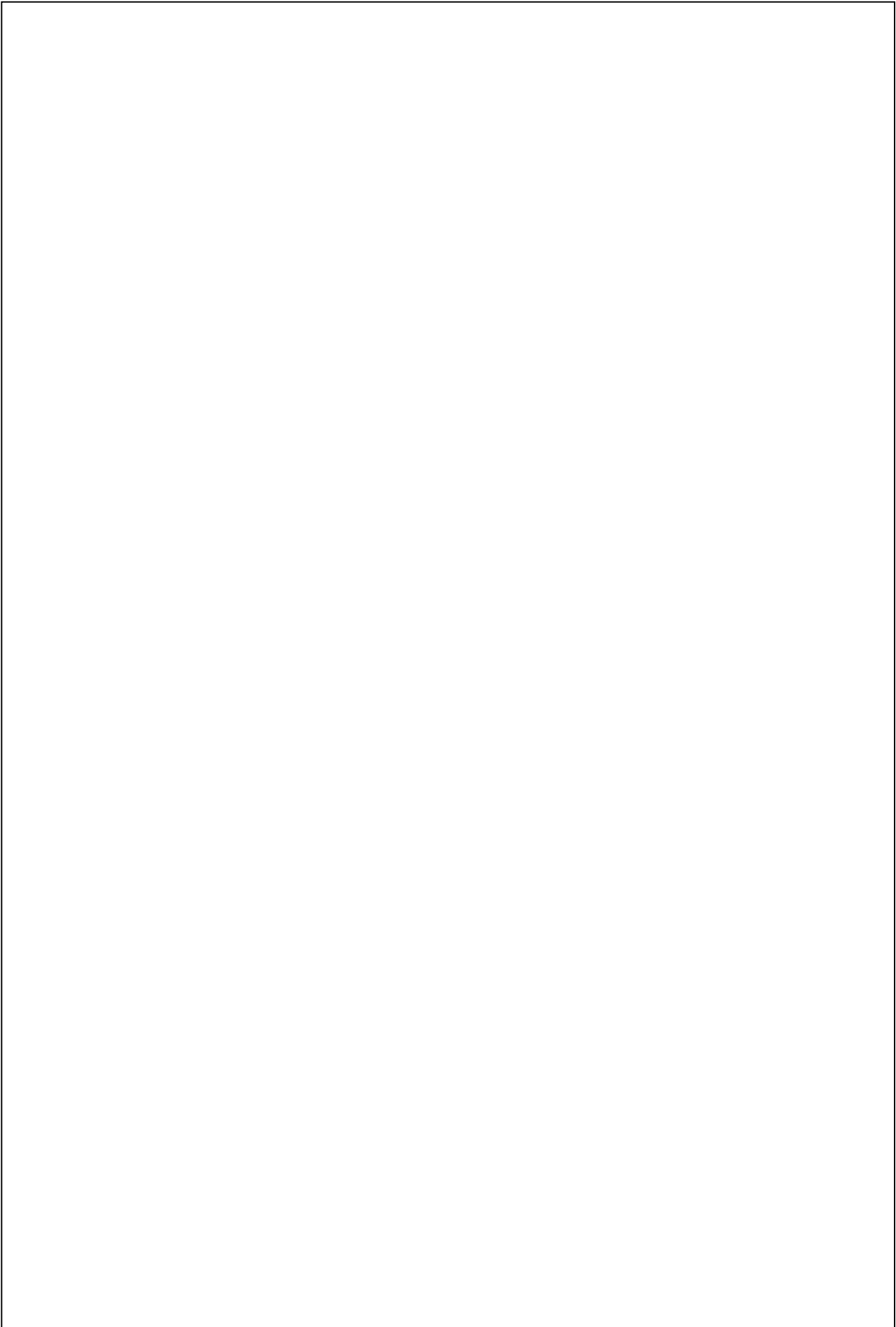
Consider a 128KB of data in a direct-mapped cache with 16 word blocks. Determine the size of the tag, index and offset fields if a 32-bit architecture (ie. 32 address lines) is employed and memory is only word addressable. Redo the calculation if memory is byte addressable.

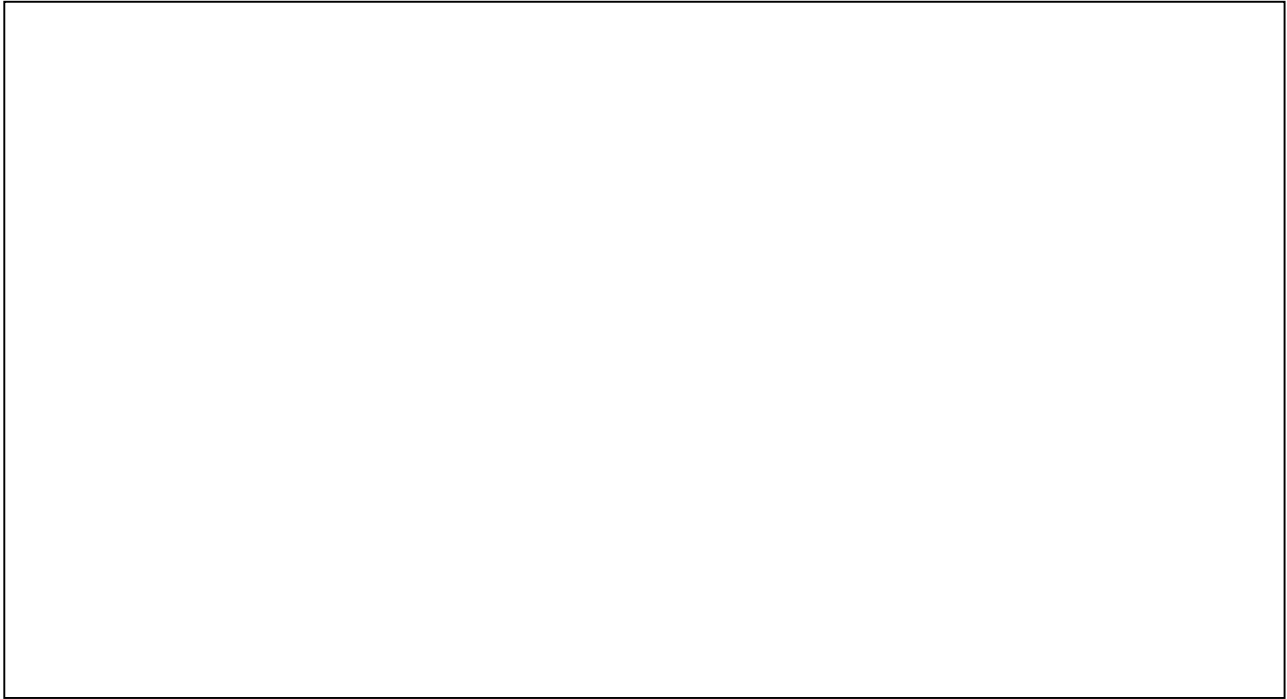


Problem 2: Data Access in Direct Mapped Cache

Consider a 128KB of data in a direct-mapped cache with 16 word blocks, for a 32-bit address architecture and word addressable memory. Analyse the data access pattern to memory and cache for the accesses to memory locations 0x00000014, 0x0000001C, 0x000001F4, and 0x8000002C.



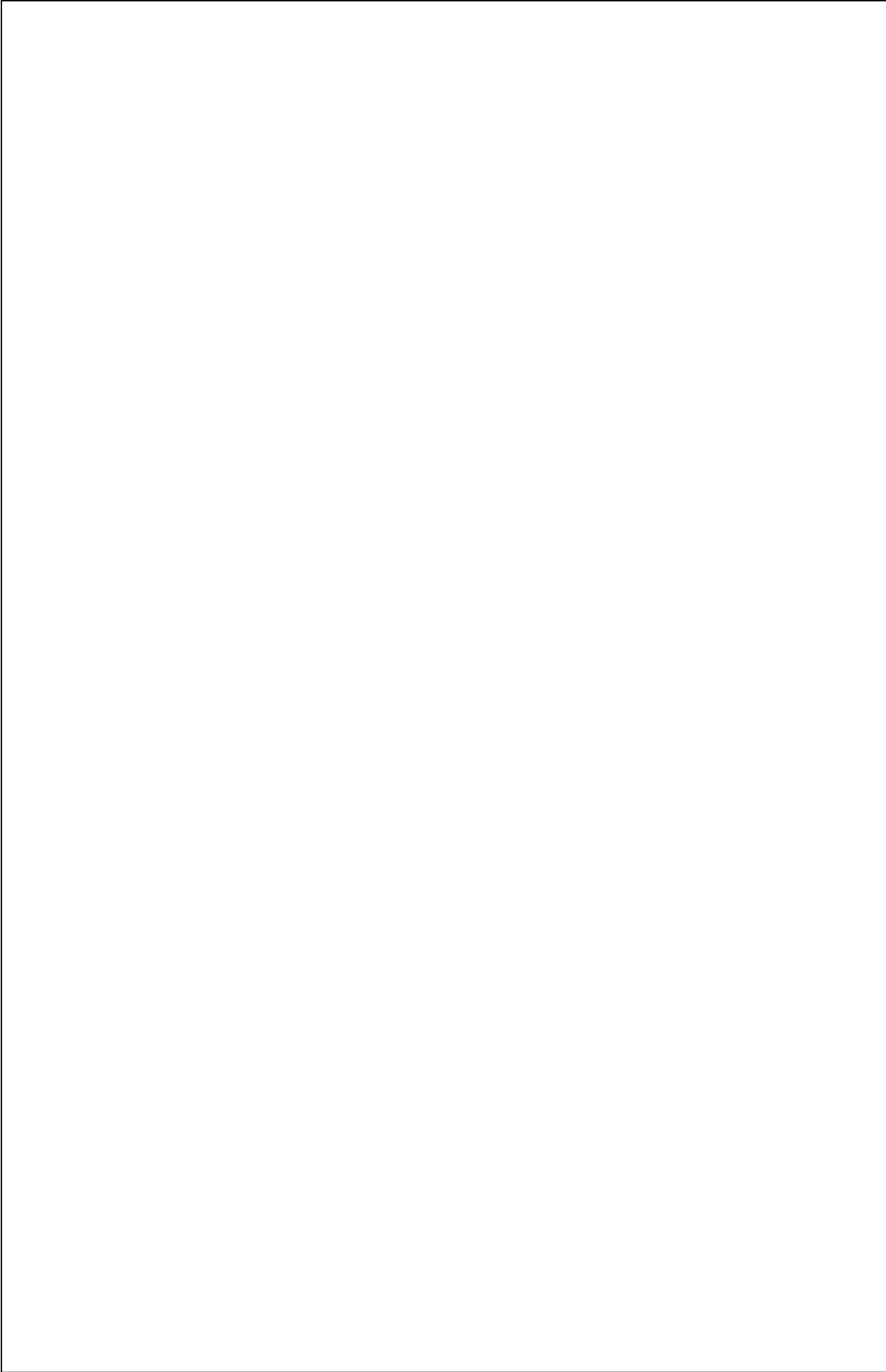




Problem 3: 2-Way Set-Associated Cache

Consider a 128KB of data in a 2-way set associative cache with 16 word blocks. Determine the size of the tag, index and offset fields if a 32-bit architecture (ie. 32 Address lines) is employed and memory is only word addressable. Redo the calculation if memory is byte addressable.





Problem 4: Multi-level Cache

Assume a 2-level cache system with the characteristic below. Compute the average the memory access time.

L1 Hit Time = 1 cycle

L1 Miss Rate = 2.5%

L2 Hit Time = 6 cycles

L2 Miss Rate = 17% (% L1 misses that miss)

L2 Miss Penalty = 120 cycles

