Electronics Topic: Supplementary Tasks

This supplementary design task is provided for students who obtained less than 42.5/85 in the Electronics Topic overall, or who did very poorly in Task 4 of the Electronics topic. The supplementary task is similar to Task 4, but may be undertaken only in Week 13. Below is a detailed explanation of the conditions under which you can undertake this supplementary task and the maximum marks that you may be able to achieve for it.

Condition A: If you obtained less than 42.5/85 overall in the Electronics topic, you may undertake the supplementary task here, regardless of how you performed in Task 4. All marks obtained in the supplementary task will be added to your existing score up to a maximum of 43/85.

Condition B: If you did not undertake Task 4, or you performed poorly in that task, obtaining a performance score (out of 12) that was no larger than 8, you may undertake the supplementary in this document. In this case, your performance score for Task 4 will be modified to the smaller of 8 and the performance score you obtain in the supplementary task, unless this is smaller than your original Task 4 performance score. The same will be done for your understanding mark in Task 4, up to a maximum of 6 understanding marks, but only if you meet the performance requirement for the task.

If both of the above conditions apply to you, both methods for updating your Topic 1 score will be used and the larger of the two marks will be taken. The first condition allows you to potentially obtain the most marks from the supplementary task, but caps the result at 43, while the second condition limits the marks you can get for the task but applies no cap to your total.

If your score from Topic 1 was extremely low, so that there are insufficient supplementary marks available to bring your score to the half way mark, you should still undertake the supplementary task to the very best of your ability. Failure to do so will be indicate a lack of commitment to the course outcomes.

Your breadboard **may not be populated prior** to the laboratory session in Week 13 – demonstrators will insist upon this. Also, you may not bring any notes into a laboratory session other than printouts of materials from the class web-site and **written notes from a previous laboratory, duly signed off in your laboratory notebook.**

Sharing Equipment and Communication in the Lab

Due to equipment constraints, you will generally share a work bench in the laboratory with a lab partner. Despite this, your design, implementation and assessment for these tasks are all individual. Naturally, you cannot expect to have your design permanently tethered to the power supply, oscilloscope, signal generator or other laboratory equipment. You should, therefore, communicate with your lab partner and establish a good working relationship for sharing the equipment.

No other communication is allowed during the supplementary laboratory. **Demonstrators have full authority to clamp down on unnecessary communication**, including by moving troublesome students to the end of the assessment list.

Assessment Procedure

Demonstrators will maintain an ordered assessment list. You may not add your name to the list until you have a solution you are prepared to have assessed. Students who have already been assessed for the supplementary task may still have the opportunity to be re-assessed, but students who have not yet been assessed will be given priority over those seeking re-assessment.

Demonstrators may ask you to move to a separate area for assessment, so that your lab partner need not be disturbed. With this in mind, you should ensure that your implementation is as portable as possible, so that you can easily connect it to a separate power supply, signal generator and/or oscilloscope, as appropriate.

Supplementary Design Task

In this design task, you are to design a voltage controlled oscillator. The output voltage waveform is required to be triangular. The oscillator should adjust its frequency in response to an input control signal whose voltage ranges from 1V to 4V. The input impedance of the control terminal should be no less than 10kΩ and the output impedance of the oscillator should be no more than 1kΩ.

The minimum specified control input voltage of 1V should produce a waveform with frequency f_L, while the maximum specified input voltage of 4V should produce a waveform with a higher frequency f_H. The actual values of f_L and f_H will be given to you at the start of the laboratory session.

You may use the laboratory power supplies to power your designed circuit and you may use the signal generator to set the input control voltage, but not for any other purpose.

In addition to the hard requirements, which are stated above, your soft objective is to arrange for the triangular waveform to be as symmetric as possible. A sawtooth waveform can be considered triangular, but highly non-symmetric. A symmetric triangular waveform should have equal rise and fall times, each occupying half of the period of the oscillator.

Available Electronic Components (on hand with your lab demonstrator):

Transistors: BC549, BC559, BD139, BD140
Analog IC's: LM324, LM348, LM741, DG441/2
Digital IC's: 74LS00, 74LS74, 74LS86, 74LS123, 74LS161/3
Diodes: 1n4148
Resistors and capacitors, as found in the laboratories

Assessment for this task:

Marks for this task are as follows:

- Achievement of requirements: (____/8)
- Symmetry of the triangular waveform: (____/10)
- Understanding and neatness of the breadboard layout: (____/7)