Electronics Topic: Design Tasks 4-5

The Electronics Design topic in this subject is spread over 3 weeks, with laboratories in Weeks 1, 2 and 3. This handout introduces design tasks 4 and 5 within this topic. The final task 6 for this topic will be released released according to the schedule that appears on the course web-page at http://subjects.ee.unsw.edu.au/~elec4123.

Your performance in these design tasks will be assessed in the laboratory, although your participation in tutorial discussions will be separately assessed (worth a total of 20% over the duration of the course). The laboratory component of your assessment for the electronics design tasks as a whole is worth 17% of the marks for the course. As indicated in the course overview, this is composed of 10% for design outcomes and 7% for understanding. To simplify the awarding of marks, these percentages are multiplied by a factor of 5. This means that there are a total of 50 marks for design outcomes in electronics and 35 marks for design understanding in electronics. An individual breakdown of the maximum marks available for each task is provided in the following. However, these individual figures may add up to more than a total of 85 marks. Where this happens, your overall mark in the electronics design topic will be capped at 85.

Note carefully that your breadboard **may not be populated prior** to any laboratory session – demonstrators will insist upon this. Also, you may not bring any notes into a laboratory session other than printouts of materials from the class web-site and **written notes from a previous laboratory, duly signed off in your laboratory notebook.**

You will, however, be **permitted to take your populated breadboard** and any electronic components which you have used out of the laboratory, for your own independent experimentation. However, components must be signed off by the demonstrator and you must bring these same components back to the laboratory the following week, together with an unpopulated breadboard.

Sharing Equipment and Communication in the Lab

Due to current resource constraints, you will generally share a work bench in the laboratory with a lab partner. Despite this, your design, implementation and assessment for these tasks are all individual. Naturally, you cannot expect to have your design permanently tethered to the power supply, oscilloscope, signal generator or other laboratory equipment. You should, therefore, communicate with your lab partner and establish a good working relationship for sharing the equipment.

Although assessment is individual, you can communicate freely with your lab partner regarding the design problem. There is no expectation that your partner should help

you with the construction of preliminary testing of your design, but this is permitted so long as you both agree.

Apart from communication with your lab partner and the lab demonstrators, you should avoid any significant communication with other students in the lab. **Demonstrators have full authority to clamp down on unnecessary communication**, including by moving troublesome students to the end of the assessment list, which may delay assessment until a following week – you will find that being assessed early is very important for success, especially since you are not permitted to bring assembled solutions into the laboratory.

Assessment Procedure

Demonstrators will maintain an ordered assessment list. You may not add your name to the list until you have a solution you are prepared to have assessed. Students who have already been assessed for a task may have the opportunity to be re-assessed, during the same or a later laboratory session, but students who have not yet been assessed will be given priority over those seeking re-assessment.

Demonstrators may ask you to move to a separate area for assessment, so that your lab partner need not be disturbed. With this in mind, you should ensure that your implementation is as portable as possible, so that you can easily connect it to a separate power supply, signal generator and/or oscilloscope, as appropriate.

Electronics Design Task 4

In this design task, you are to design a voltage controlled oscillator. The output voltage waveform is to be periodic, but its shape is up to you (square wave, triangular wave, sinusoidal, etc.). The oscillator should adjust its frequency in response to an input control signal whose voltage ranges from 1V to 2V. The input impedance of the control terminal should be no less than 10kΩ and the output impedance of the oscillator should be no more than 1kΩ. The minimum specified control input voltage of 1V should produce a waveform with frequency f_L, while the maximum specified input voltage of 2V should produce a waveform with a higher frequency f_H. The actual values of f_L and f_H will be given to you at the start of the laboratory session. You may use the laboratory power supplies to power your designed circuit and you may use the signal generator to set the input control voltage.

As with this all the design problems, there are many solutions, which may look quite different. You are strongly encouraged to discuss the design requirements and possible solutions in your tutorial group.

In addition to the hard requirements, which are stated above, design problems usually have soft objectives which are desirable to optimize. For this particular design task, your soft objectives are: 1) to come up with a design which is as simple and elegant as possible; and 2) to minimize the need for experimental calibration of the circuit – that is, the performance should not be overly sensitive to manufacturing variations between components.

Available Electronic Components (on hand with your lab demonstrator):

Transistors: BC549, BC559, BD139, BD140
Analog IC's: LM324, LM348, LM741, DG441/2
Digital IC's: 74LS00, 74LS74, 74LS86, 74LS123, 74LS161/3
Diodes: 1n4148
Resistors and capacitors, as found in the laboratories

Assessment for this task:

Marks for this task are as follows:

- Achievement of requirements: (____/10)
- Elegance and insensitivity to manufacturing tolerances: (____/2)
- Understanding and neatness of the breadboard layout: (____/7)

Weeks in which this task may be completed:

You may complete this task in any of Weeks 2 or 3. However, the parameters f_L and f_H will generally change from week to week, which may possibly require you to modify your design approach.

Electronics Design Task 5

In this design task, you are to design a digital circuit which can divide its input clock frequency by an integer value D. The value of D will be given to you at the start of the laboratory session. The input to the divider may be taken as a square wave with TTL voltage levels. For the purpose of testing, you may take the input from the TTL output of the signal generators in the laboratory, but you could also base your input on your solution to Task 4. The output from your circuit should also be a square wave with TTL voltage levels although the duty cycle may be as small as 1:D-1.

As with all design tasks, you are strongly encouraged to discuss possible solutions to this problem in your tutorial group.

Your soft design objective for this task is to find the simplest circuit which achieves the design objectives. This will, in general, depend upon the value of D. The design does not need to be flexible enough to accommodate dynamically changing the value of D.

Available Electronic Components (on hand with your lab demonstrator):

Transistors: BC549, BC559, BD139, BD140
Analog IC's: LM324, LM348, LM741, DG441/2
Digital IC's: 74LS00, 74LS74, 74LS86, 74LS123, 74LS161/3
Diodes: 1n4148
Resistors and capacitors, as found in the laboratories

Assessment for this task:

Marks for this task are as follows:

- Achievement of requirements: (____/5)
- Elegance (i.e., simplicity) of the design: (____/3)
- Understanding and neatness of the breadboard layout: (____/5)

Weeks in which this task may be completed:

You may complete this task in any of Weeks 2 or 3. However, the parameter D will generally change from week to week, which may possibly require you to modify your design approach.