Organization and Marking of the Elective Design Topics (General)

The elective design topics are all undertaken between Weeks 10 and 12 in the laboratory. Unlike the core design topics, the elective topics are undertaken by a team of 3 or (preferably) 4 students. Some of the marks are awarded to the team as a whole, while others are awarded individually.

It is highly desirable for all students in an elective design team to belong to the same tutorial group. While this might not always be achievable, the following factors should be considered when forming teams:

1. There will be no rearrangement of tutorial membership to accommodate the elective design topics. Each student is expected to attend his/her originally assigned tutorial, regardless of elective design team membership.
2. During the tutorials in Week 11 and Week 12, students are expected to discuss ideas, problems and their understanding of the elective design topic they are working on.
3. Roughly half of the tutorial time will be spent discussing these matters in a team huddle. The other half of the tutorial time will be spent exchanging ideas and problem understanding between teams. This requires students to be competent in explaining the design problem that their team faces; it also requires students in other teams to pay close attention and contribute useful suggestions or clarifying questions. It is expected that this monitored interaction between design teams will bring considerable benefits to learning and outcomes.
4. If a team of (say) 4 students is split across two tutorial groups, the responsibilities outlined above effectively become more challenging for the individual students. For example, if only 2 students from a team belong to a given tutorial, they become fully responsibility for explaining the problems and progress of their team to the tutorial. It is not sufficient for individual team members to be familiar only with some aspect of the work that is their primary responsibility. All students in each elective design team need to be familiar with the problems and approaches being employed by the entire team.

As with the other design topics, your individual participation in tutorials is assessed separately and contributes to the tutorial component of your final mark (20% over the duration of the course).

The laboratory component of your assessment for the elective design topics is worth 17% of the marks for the course. This is represented by a mark in the range 0 to 85, which consists of two components: a design outcomes component (up to 50 marks); and an understanding component (up to 35 marks). The design outcomes component is awarded to the team as a whole, whereas the understanding component is individually

assessed. All assessment of the laboratory component of the elective design topics takes place in Week 12 only.

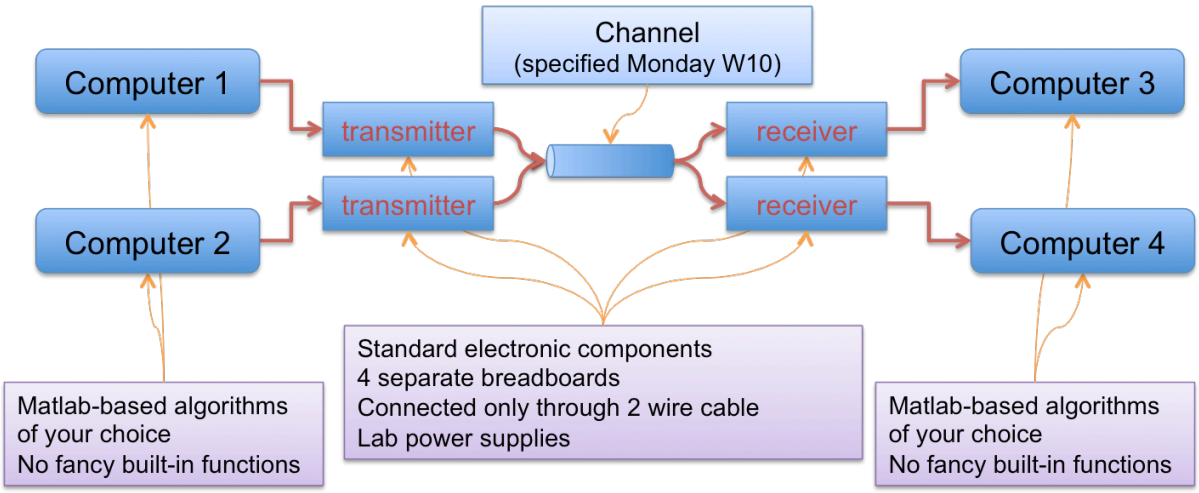
Additionally, 12% of your assessment for the course as a whole is based upon a report that you write as a team and submit by email to d.taubman@unsw.edu.au, no later than 5pm Thursday in Week 13. A draft version of the report must be available from the start of the laboratory session in Week 12. This will form part of the basis for assessment of understanding, as individual team members are interviewed.

An overview of the report structure may be found on the course web-site. Two particularly important elements are the high level decomposition of the design problem into tasks, assigned to individuals, and the technical documentation of each of the design tasks (managed by the individual to whom they have been assigned).

Physical Communications Design Topic

Context and Objectives

The objective of this design project is to reliably communicate information between two pairs of computers, over a shared "channel". Your tasks are to design and build two separate transmitters whose outputs are added and delivered over a shared channel, along with two separate receivers, which derive their data from the output of the shared channel. The configuration is illustrated below:



The "channel" consists of two bread-boards, connected via a shielded cable. The first breadboard implements an opamp summing amplifier, while the second breadboard implements filtering, a noise source and two opamp buffers, to drive the receivers. This second breadboard will be provided for you, along with the shielded cable and specifications; note that the second breadboard's filter will not pass DC. The first breadboard **(the summing amplifier) is something that you must specify and provide.**

Computer 1 and Computer 2 will be loaded with separate messages, consisting of plain ASCII text. Your designed system must communicate the message on Computer 1 to Computer 3 and the message on Computer 2 to Computer 4, with 100% reliability. The soft measure of performance for this topic is the time taken for Computers 3 and 4 to report that they have successfully received their respective messages.

Constraints

Each transmitter and each receiver must be implemented on its own breadboard (or multiple breadboards) and connected to its respective computer. The only wires which these breadboards may share with each other and the summing breadboard are ground and up to two power rails, from the laboratory power supplies.

You may use up to four signal generators if you like. You may also use multiple power supplies, but be aware that the power supply outputs are all floating.

You may use any of the "standard" electronic components which have been made available for any of the core design topics in this course – these are also listed on the course web-site.

The computers may not communicate with each other by any means other than the transmitter and receiver circuits which you design, driven by algorithms that you implement using Matlab. You may not use "complex" Matlab built-in functions – nothing more complex than FFT's and convolution. If in doubt, ask permission!

Design Outcome Marks

The hard requirement for this project is that you must be able to communicate the messages with 100% reliability, even if this takes a long time. This is reflected in the marking scheme. The second basis for the marking scheme is the time taken for both receiving computers to recover the message (without errors) – this is measured in terms of the average character rate. Averaging may be performed over multiple trials. Finally, the marking scheme reflects the general desirability of an elegant design, where simpler approaches are preferred unless a complex solution brings clear benefits.

Your design outcome marks will be awarded as follows:

- Both messages communicated with 100% reliability: (____/15)
- Message transfer time (full marks for X chars/s, X to be provided): (____/15)
- Design principles, elegance, etc.: (____/12)
- Neatness of hardware and clarity of code (must meet objectives first): (____/8)

Note: In the event that your design exceeds the transfer speed target of **X** chars/s, bonus marks may possibly be awarded to compensate for less than perfect performance in other assessment criteria associated with this design topic.

Understanding Marks

- Understanding of system design, trade-offs and choices: (____/10)
- Understanding of individual sub-systems designed: (____/15)
- Understanding of how things could be further improved: (____/10)

Note: the first two items mentioned above must be supported by the draft report provided in the laboratory in Week 12. The draft report must contain at least a close approximation to the final Matlab code and designed circuits. Lab notebooks and print-outs must provide remaining details by the time of marking.