From: **David Taubman** d.taubman@unsw.edu.au
Subject: Open Lab, suggestions and observations for Topic 1
Date: 10 March 2017 at 1:04 PM
To: ELEC4123@ee.unsw.edu.au

Dear Students,

As announced in the laboratory yesterday, I have some valuable information to share with you here. I will also put a copy of this email on the subject web-site at http://subjects.ee.unsw.edu.au/~elec4123 in case any of you miss the email.

Open Labs

Some students have asked us if we could provide an open lab session, to assist you in preparing for your assessed laboratory sessions. While this is not always simple to achieve, I have managed to secure an open lab for the coming Wednesday, from 5pm to 8pm, which is available to all students in ELEC/TELE/PHTN4123. At a minimum we will open EE101/102, but we might also be able to open other laboratories as the need arises.

Please note that you may not be assessed during the Open Lab. The primary role for the two demonstrators I have assigned to this lab is to maintain order and security within the lab. However, time permitting, it may be possible for them also to answer technical questions.

Also, you will not be able to obtain any of the standard components during the open Lab, with the exception of resistors and capacitors commonly available in the lab.

If space is insufficient, you may need to share equipment, and you should be generous in the way you do this. Please, also be respectful of others in not collecting any more cables than you absolutely need, and make sure you **tidy up afterwards**. If you do not do this, we may not be able to offer other such open labs in the future.

If this is successful, we may create Open Lab sessions for later topics in the course also.

Sharing of Cables

In both Week 1 and Week 2, the availability of cables has been a problem in the labs, to varying degrees. The reality is that the labs are equipped with more than sufficient cables to accommodate all the equipment on the benches -- this means 3 BNC cables and 6 power cables per bench position. This allows for one signal generator channel, two oscilloscope channels, four power outputs and two multi-meter inputs. There is no good reason why more than this number of cables should be required, although the labs do have additional cables to cover problems that may occur.

It has come to my attention that the cabling problem is mostly due to students individually collecting cables for their design, which of course can lead to an over-demand of cables by up to a factor of 2. This is not appropriate. The cables belong to the equipment, not to your design. When you test your implementation, the right approach is to attach the cables that are already associated with the equipment to your design at that point. You should never use laboratory cables as part of your design, especially because you will usually move to one of the assessment benches to demonstrate your design. When moving to an assessment bench, you should use the equipment cables at the assessment bench, since the whole point of this is to leave your partner free to continue using the equipment.

In some cases, students are collecting extra cables to inter-connect the power supply outputs externally. You should not do this. All of the power supplies are equipped with buttons that control the inter-connection of output terminals internally, and this is the reliable and efficient way to generate common configurations, such as a double-ended supply. If you have any doubts on how to do this, you may consult the demonstrator.

Approach to Design

I have noticed that at least some students (probably many) are adopting a trial-and-error approach to design. This is quite possibly a hang-over from earlier years, where design intensive courses may have been introduced before you had a thorough grounding in the principles. However, this method is extremely unreliable, often leading to designs that depend upon the behaviour of a specific manufactured component for which there is no guarantee of consistency. More importantly, design by trial-and-error is very slow and ultimately entirely infeasible once the design problem becomes more complex.

In short, you cannot get away with this method.

A clear sign that you may be using the trial-and-error method is that you are not reading the data sheets for the components you are using. For example, a massive number of students are designing solutions to the tasks using op-amps, without having any idea what the common-mode voltage range, output current limitations, slew rate limitations or supply requirements for the op-amp actually are. This is particularly problematic, because the design parameters often challenge one or another of these attributes.

In some cases, a solution works, but for all the wrong reasons, so that taking the design further becomes impossible; even swapping a different component into the implementation may entirely break some solutions.

Tips and Suggestions for Week-3

1. You do not need to be assessed for one task at a time, nor do you need to get the tasks assessed in sequence.

2. Please note that **Task 5 is extremely do-able**. The harder tasks are Task 4 and Task 5, so be sure not to miss out on assessment for Task 5.

3. Understanding marks can be given even if your design does not yet work, so **document your designs very carefully in your lab notebook** to make it easier for demonstrators to award you an understanding mark for a task where things might not yet work.

4. Many of you are using very small breadboards, which is **a huge mistake**! With a larger breadboard you can assemble solutions to multiple tasks and get them marked together. This will save a massive amount of time. If you have started out with a small breadboard and you wish to change to a larger one in Week 3, bring your old and new breadboards to the lab so that the demonstrator can verify your stickers if required.

5. Some of you have noticed that the tasks are building upon each other. It should come as no surprise when the solution to an earlier task winds up forming a part of a good solution to a later task.

6. In each of the tasks there has been some kind of optimization target, associated with bonus marks. Some of you might not have been paying any attention to this, but it can be used as a hint. In each case, the selected optimization target is there because the simplest or most obvious solution has some limitation of the form identified in the optimization target, so this can actually be interpreted as a hint as to how to answer the question "what is the hard part of this task?" Recall that this is a fundamental question you should always ask yourself as you start and throughout the process of designing a solution to a problem -- that is the essence of a "problem statement."

Good Luck in Week 3!!

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Professor David Taubman
Deputy Head of School (Research)
School of Electrical Engineering and Telecommunications
UNSW Sydney,
NSW 2052, Australia

Email: d.taubman@unsw.edu.au
Phone: +61 2 9385 5223