# ELEC 4123: Design Proficiency
# Session 1, 2018

Introduction to the Course

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# Overview of 4123

- Objectives:
  - Ensure that you have a minimum level of proficiency
    - Testing!!
  - Plug major holes in your knowledge
  - Increase your confidence
  - Prepare you to make a valuable contribution in the work force

# How it Works

- Lectures: W1-5, W7-10
- Labs: every week
  - 75% of your assessment is in labs
- Tutorials: W11-13 (during lecture timeslot)
  - 10% of your assessment comes from these
- Written reports: due after Week 13
  - 15% of your assessment comes from a group report

# Design Topics

- Core (individual):
  - Electronics (3 weeks)
  - Signal Processing (3 weeks)
  - Control (3 weeks)
- Elective (final 3 weeks, done in Teams of 4):
  - Energy systems
  - Telecommunications
  - Data networks
  - NB: Part of the assessment here is still individual

# What you need

- A bound lab notebook at every lab
- A breadboard
  - preferably large, or use two smaller ones
  - bring the same ones to every lab
- A small screwdriver
  - for adjusting trimpots
- Shoes – you know the drill
- Your witts
  - every lab is a bit like an exam
- Consideration for others
  - there should not be much in-lab conversation
  - don’t take more cables/parts than you need

# The Big Question

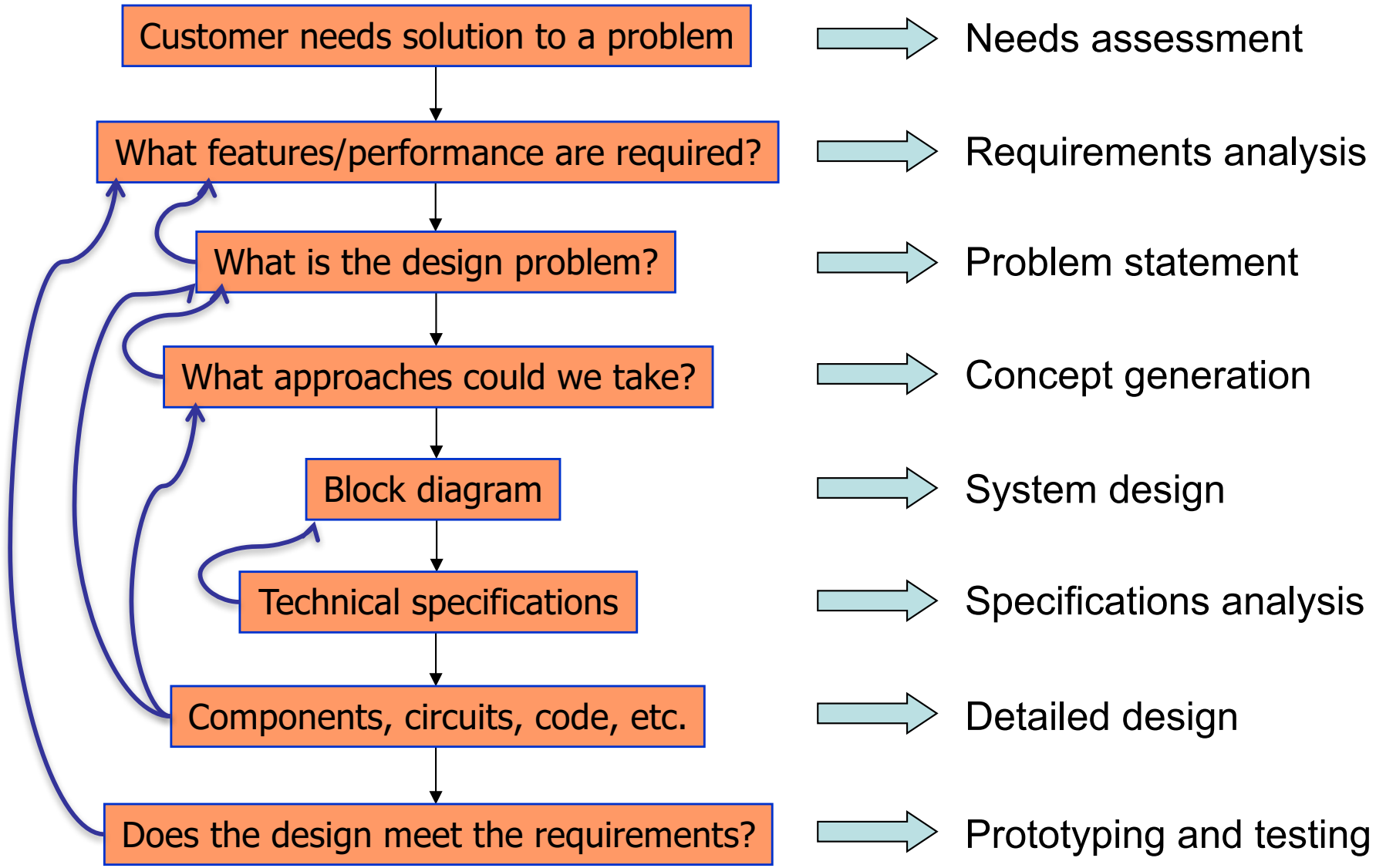
- What happens if I fail a topic?
  - Do not panic
  - I do not want you to fail the course
  - I do want you to get as much as possible out of it
  - You can make up for failing a topic by doing well in other topics
  - Marks may be scaled at the end, but
    - you should not expect to benefit from any scaling if you have not scored at least 50% over the individual components of assessment.

# What's Happening in Week 1?

- EE&T Building Refurbishment
  - laboratories are ready for use in Week 1
  - but not all of the bench equipment will be installed
- Week 1 Pre-Lab
  - demonstrators will act as mentors during this pre-lab
    - in Weeks 2-10 and 13 their primary role is assessment only
  - to prepare for the pre-lab, read Tasks 1-4 of Topic 1
  - pre-lab activity:
    - engage in brainstorming to set you on the right path
    - problem statement: "what is the most problematic aspect" of each design task ?
  - you should find this activity very helpful!
  - starts at 9am, but likely to finish well before 1pm

# BRIEF REVIEW OF DESIGN PROCESS AND TERMINOLOGY

# Typical Design Phases




*NB: Iteration is everywhere; only the more interesting paths are shown*

# Requirements, Specs, Objectives

- Requirements must be satisfied
  - May be stated in non-technical language
- Specifications characterize achieved performance
  - Technical in nature; may be derived from requirements
  - Some specifications may be determined after an initial design is complete
- Design objectives are quantities which should be optimized
  - E.g., power efficiency, communication range, usabiity, etc.

# Design Scenarios

- Consulting engineer
- New product design
- Redesign of an existing product
- System engineering
- Design of a sub-system to fit within a larger system design

# LEARNING APPROACH

# Reflective Cycle

- Each topic lasts 3 weeks
  - you should expect to get stuck in earlier weeks
  - learn from your mistakes
  - do your own research/revision between weeks
  - discuss with your peers (outside laboratory hours)
  - try again
    - you can be assessed multiple times
    - but no more than 3 tasks assessed in any week
- Elective topic is assessed only once!
- Reflect after each topic:
  - Would it have helped to spend more time asking yourself what is likely to be hardest about each task?

# Partners, Elective Teams and Tuts

- You will share equipment with a lab partner
  - but you do your own design and implementation
  - your partner and lab bench are assigned by the course convener; generally changes for each topic
- Elective topic done in teams of 4 (or perhaps 3)
  - you are still expected to know the overall design
- You will be assigned a tutorial group
  - only for the elective design topic
  - tutor can offer advice; also monitors team interaction
  - tutor will give a subjective evaluation, worth 10%

# COMMON PITFALLS

# Where the smooth path leads …
# … may be the base of a cliff

- Why is the “problem statement” part of design?
  - This is where you identify the “real problems”
  - A good problem statement includes some statement like: “The most challenging aspect of the design is likely to be …”
- Concept generation focusses on the hard bits
- Detailed design also starts with the hard bits
- Design iteration is mostly due to the hard bits
- Project management also driven by the hard bits
  - hard to know how long they will take
  - have to guess and constantly monitor progress

# How can I know what is hard?

- Takes experience and practice
  - Every design course will help / has helped you
  - This design course will help you
- Reflect:
  - At the end of each design task, ask yourself: "What really was the problem?"

# Being Precise

- You cannot do design with only a vague idea
  - The end must be concrete
- If you start with a fuzzy mental picture
  - Start drawing diagrams to make things clearer
  - Don't stay in high level La La land
    - producing a detailed design will help expose the real issues
- Use a lab notebook
  - Mandatory in this course!!!!
  - Draw schematics, flow diagrams, etc.
  - When debugging
    - sketch your circuit/code, insert numeric values, etc.
  - Record your assumptions, formulae, concerns, …

# Use what you have learned

- "Theoretical" material taught in classes
  - is actually useful
- If a problem is hard, it needs structure
  - that is what all your courses have been about
  - mathematics is about structuring a problem
  - many problems are connected by common theory
- Don't separate practice and theory
  - you cannot do the lab properly without some theory
  - you can waste your whole life looking for a solution that is already given by an elegant theory
  - most students badly miss this point

# HOW TO SUCCEED IN THIS COURSE

# Get it to work

- Quite a bit of the assessment is objective
  - Does it meet the requirements?
  - If it does not work, how can it meet any requirement?
  - 0 is a mark
  - It is not sufficient (or even helpful) to tell the demonstrator *how it was supposed to work*

# Prepare outside of the labs

- You need to do a lot of thinking outside the lab
- You have 3 weeks for each topic
  - plenty of time to reflect on problems experienced in one lab session so that you can succeed in the next
- Prepare multiple designs approaches
  - when you get into the lab you may discover a problem you never expected

# Come to in Lectures

- The intent is to for most of the lectures to be interactive in nature
- Ask questions
- Find out what to do about common problems

# Get your name on the marking list

- Once you are ready to be assessed for a task
  - let the demonstrator know
  - if you do not get marked during the lab, you may need to start all over again the following week
  - there is no point in complaining that the demonstators were too busy to mark your work
- You are allowed to be re-assessed
  - but you go onto a second (low priority) list
  - if the demonstrators are too busy, your work might not be re-assessed
  - you cannot expect to be assessed for more than 3 tasks in any given week, so plan around this

# Collaborate but do not Collude

- Exchange ideas with your peers
- You will have a lab partner
  - feel free to help each other with debugging or advice
  - but the lab partner is not your choice
- You will be individually assessed
  - individual implementation
  - individual lab notebook (handwritten)
  - individually interviewed
- The demonstrators can easily tell if you are cheating
  - if they even suspect this they can immediately drop you to the bottom of the assessment list, …
  - or deny you further assessment that week (after a warning)

# ELECTRONICS TOPIC

# 6 Tasks

- Starts simple
  - goal is to ensure proficiency
- Final task is a type of communication system
  - discriminate between two signals in (lots of) noise!
  - not all students will get there
  - but all students should at least reach task 4
- Tests your ability
  - work with analog and digital electronics
  - multiple solutions exist

# General guidelines

- All work is done on your own breadboard
- No free selection of components
  - can only use the small set of designated components
  - this is a design constraint
  - makes it harder to copy a solution you find online
- You can take out, but you cannot bring in
  - take out populated breadboard, components, lab notes
  - bring in unpopulated breadboard, any components you received last time, plus design and lab notes

# Assessment

- Tasks have different earliest assessment weeks
- All tasks can be assessed in the last week
  - but you cannot rely upon demonstrator availability
  - plan to be assessed early
  - plan to be able to have multiple tasks implemented concurrently
- Make your implementation portable
  - You may be asked to go to a set of special workbenches for assessment.